

**ABSTRACT**

A phase locked loop (PLL) is provided. In one implementation, the PLL includes a feedback loop having a frequency multiplier and an integer divider to generate a 5 divided signal. The PLL includes a re-sampling circuit operable to re-sample one or more digital pulses of the divided signal using one or more phase signals if a multiplication factor of the frequency multiplier does not divide evenly into the integer divisor.

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